








PTO/SB/08a/b (08-03)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT			Complete if Known		
(Use as many sheets as necessary)			Application Number	10/698,805	
			Filing Date	October 31, 2003	
			First Named Inventor	Szpak, Peter	
			Art Unit	2123	
			Examiner Name	Not Yet Assigned	
Sheet	1	of	1	Attorney Docket Number	MWS-058

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	A1	5,371,851	12-06-1994	Pieper, et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ³
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)	MM-DD-YYYY			

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NON PATENT LITERATURE DOCUMENTS				
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²	
	A2	Drongowski, et al. "A Graphical Hardware Design Language." <i>Proceedings of the Design Automation Conference</i> , June 12, 1988, paper 9.2, pp. 108-114.		
	A3	Lavagno, et al. "A Simulink ©-based Approach to System Level Design and Architecture Selection." <i>Proceedings of the Euromicro Conference</i> , September 5, 2000, pp. 76-83.		
	A4	May, P. "A Flexible VHDL Test Bench Architecture." <i>Military Communications Conference, IEEE San Diego, CA</i> , October 11, 1992, pp. 979-985.		
	A5	Molson, P. "Accelerating Intellectual Property Design Flow Using Simulink® for System on a Programmable Chip." <i>Conference Record of the 35th Asilomar Conference on Signals, Systems & Computers</i> , November 4, 2001, pp. 454-457.		
	A6	Mrad, et al. "Real-Time Control of Free-Standing Cart-Mounted Inverted Pendulum Using LabVIEW RT." <i>Proceedings of World Congress on Industrial Applications of Electrical Energy and 35th IEEE-IAS Annual Meeting</i> , October 8, 2000, pp. 1291-1298.		
	A7	Skahill, K. "Entities and Architectures." <u>VHDL for Programmable Logic</u> . Cypress Semiconductor, Addison Wesley, Menlo Park, CA, 1996, pp. 105-158.		
	A8	Skelly, et al. "A LabVIEW Approach to Instrumentation for the TFTR Bumper Limiter Alignment Project." <i>Proceedings of the IEEE/NPSS Symposium on Fusion Engineering</i> , September 30, 1991, pp. 765-768.		

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¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

Examiner Signature		Date Considered	2/6/2007
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PTO/SB/08a/b (07-05)

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Substitute for form 1449A/B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Complete if Known			
		Application Number	10/698805-Conf. #2494		
		Filing Date	October 31, 2003		
		First Named Inventor	Peter SZPAK		
		Art Unit	2123		
		Examiner Name	Not Yet Assigned		
Sheet	1	of	1	Attorney Docket Number	MWS-058

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FOREIGN PATENT DOCUMENTS						
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	C1	Drongowski, Paul J., et al., "A graphical hardware design language," <i>Proceedings of the Design Automation Conference, Anaheim, June 12-15, 1988, Proceedings of the Design Automation Conference (DAC), New York, IEEE, US, Vol. Conf. 25, 12 June 1988, pp. 108-114</i>	
	C2	Lavagno, L., et al., "A Simulink®-based Approach to System Level Design and Architecture Selection," <i>Euromicro Conference, 2000. Proceedings of the 26th Sept. 5-7, 2000, Los Alamitos, CA, USA, IEEE Comput. Soc., US, Vol. 1, 5 Sept. 2000, pp. 76-83</i>	
	C3	May, Phil, "A Flexible VHDL Test Bench Architecture," <i>Military Communications Conference, 1992. MILCOM '92, Conference Record. Communications - Fusing Command, Control and Intelligence, IEEE, San Diego, CA, USA, Oct. 1992, New York, NY, USA, IEEE, US, 11 October 1992, pp. 979-985</i>	
	C4	Molson, Philippe, et al., "Accelerating intellectual property design flow using Simulink® for system on a programmable chip," <i>Conference Record of the 35th Asilomar Conference on Signals, Systems & Computers, Pacific Grove, CA, Nov. 4-7, 2001, Asilomar Conference on Signals, Systems and Computers, New York, NY: IEEE, US, Vol. 1 of 2, Conf. 35, 4 November 2001, pp. 454-457</i>	
	C5	Mrad, Fouad, et al., "Real-Time Control of Free-Standing Cart-mounted Inverted Pendulum using LabVIEW RT," <i>Proceedings of World Congress on Industrial Applications of Electrical Energy and 35th IEEE-IAS Annual Meeting, Vol. 2, 8 October 2000, pp. 1291-1298</i>	
	C6	Skahill, Kevin, "VHDL for Programmable Logic - Chapter 3, 'Entities and Architectures,'" <i>Cypress Semiconductor, Addison, Wesley, Menlo Park, CA, USA, pp. 105-158 (1996)</i>	
	C7	Skelly, G.N., et al., "A LabVIEW Approach to Instrumentation for the TFTR Bumper Limiter Alignment Project," <i>Proceedings of the IEEE/NPSS Symposium on Fusion Engineering, San Diego, Sept. 30 - Oct. 3, 1991, New York, IEEE, US, Vol. 2 Symp 14, 30 Sept. 1991, pp. 765-768</i>	
	C8	International Search Report Application No. PCT/US2004/034904, dated November 11, 2005	

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Examiner Signature		Date Considered	2/7/2007
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